ABSTRACT OF THE DISCLOSURE

A voltage level shifter is provided. The shifter includes an AND gate for generating a synchronizing signal according to a periodic signal and a primitive input signal. The synchronizing signal and a first periodic control signal that are in phase with the periodic control signal are inputted to a transistor device. The transistor device is constructed with an inverter. The voltage level shifter further includes a buffer for generating an output signal and a capacitor for storing a signal. The present invention also provides a switching circuit for preventing the turning on of both PMOS transistor and NMOS transistor simultaneously during a switching status. The present invention can also solve the issue caused by the ratio of the channel width to the channel length, thus the uncertainty of the manufacturing process will not affect the circuit. Therefore, the power consumption, the chip area and the cost are reduced.